LM5035A/LM5035A-1 PWM Controller with Integrated Half-Bridge and SyncFET Drivers

Check for Samples: LM5035A

FEATURES

- **105V / 2A Half-Bridge Gate Drivers**
- **Synchronous Rectifier Control Outputs with Programmable Delays**
- **High Voltage (105V) Start-up Regulator**
- **Voltage mode Control with Line Feed-Forward and Volt • Second Limiting**
- **Resistor Programmed, 2MHz Capable Oscillator**
- **Patent Pending Oscillator Synchronization**
- **Programmable Line Under-Voltage Lockout**
- **Line Over-Voltage Protection**
- **Internal Thermal Shutdown Protection**
- **Adjustable Soft-Start**
- **Versatile Dual Mode Over-Current Protection with Hiccup Delay Timer**
- **Cycle-by-Cycle Over-Current Protection**
- **Direct Opto-Coupler Interface**
- **5V Reference Output**

PACKAGES

- **HTSSOP-20**
- **WQFN-24 (4mm x 5mm)**
- **HTSSOP-28 (LM5035A-1 only)**

DESCRIPTION

The LM5035A Half-Bridge Controller/Gate Driver contains all of the features necessary to implement half-bridge topology power converters using voltage mode control with line voltage feed-forward. The LM5035A is a functional variant of the LM5035 half-bridge PWM controller. The VCC current limit threshold has been increased to 35 mA. The soft start and soft start currents have been increased from 50 µA to 100 µA. The BST UV threshold has been lowered to less than the VCC UV threshold. The ratio of the T1 and T2 delays on the SR1 and SR2 outputs has been increased from 2:1 to 3:1. The floating high-side gate driver is capable of operating with supply voltages up to 105V. Both the high-side and low-side gate drivers are capable of 2A peak. An internal high voltage startup regulator is included, along with programmable line undervoltage lockout (UVLO) and overvoltage protection (OVP). The oscillator is programmed with a single resistor to frequencies up to 2MHz. The oscillator can also be synchronized to an external clock. A current sense input and a programmable timer provide cycle-by-cycle current limit and adjustable hiccup mode overload protection. The differences between LM5035, LM5035A, LM5035B, and LM5035C are summarized in Table 2.

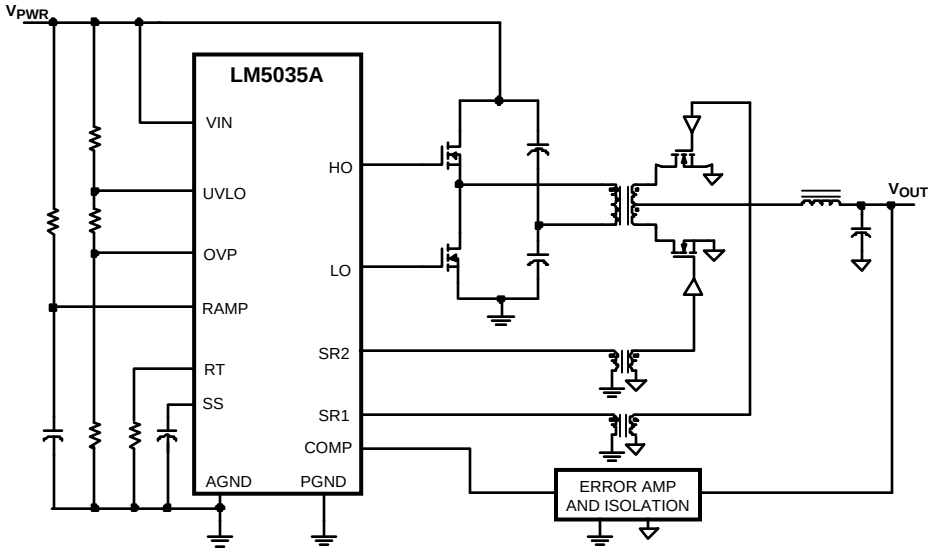
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Simplified Application Diagram



Connection Diagram

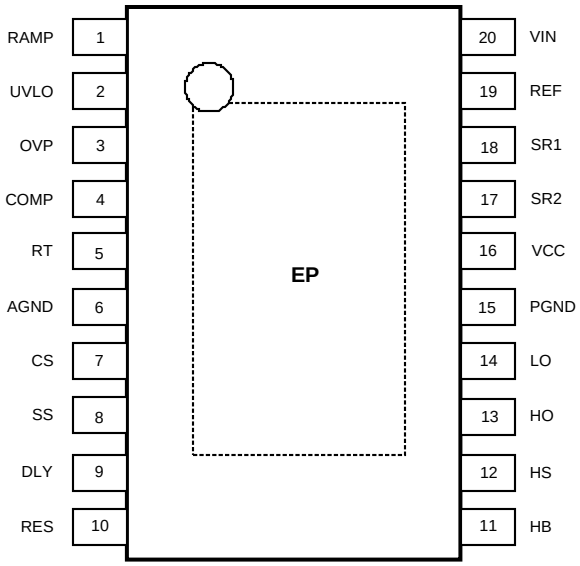


Figure 1. LM5035A
20-Lead HTSSOP
(Top View)

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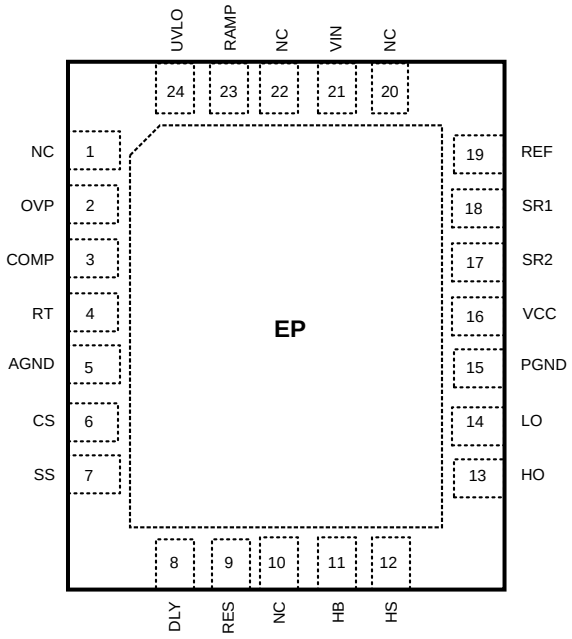


Figure 2. LM5035A
20-Lead HTSSOP
(Top View)

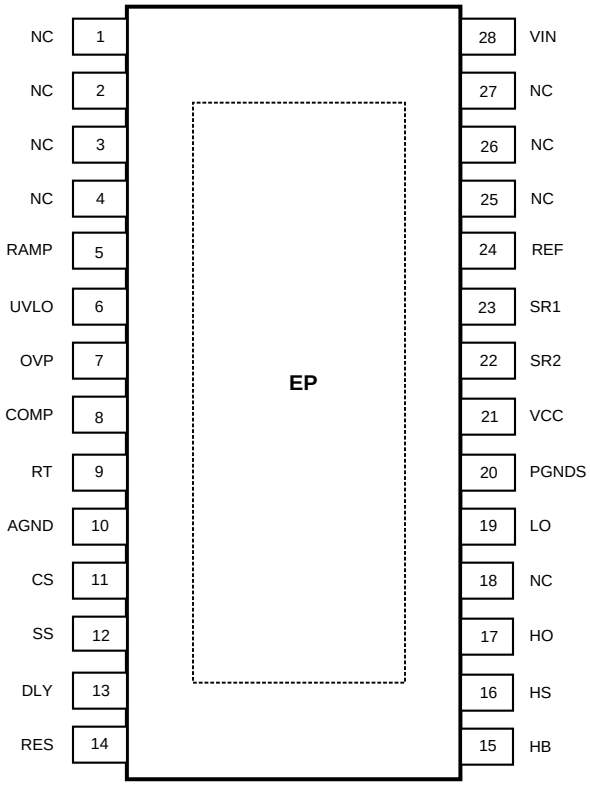


Figure 3. LM5035A–1
28-Lead HTSSOP
(Top View)

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Pin Descriptions for LM5035A and LM5035A–1

HTSSOP 20 PIN LM5035A	WQFN PIN LM5035A	HTSSOP 28 PIN LM5035A-1	Name	Description	Application Information
1	23	5	RAMP	Modulator ramp signal	An external RC circuit from VIN sets the ramp slope. This pin is discharged at the conclusion of every cycle by an internal FET. Discharge is initiated by either the internal clock or the Volt • Second clamp comparator.
2	24	6	UVLO	Line Under-Voltage Lockout	An external voltage divider from the power source sets the shutdown and standby comparator levels. When UVLO reaches the 0.4V threshold the VCC and REF regulators are enabled. When UVLO reaches the 1.25V threshold, the SS pin is released and the device enters the active mode. Hysteresis is set by an internal current sink that pulls 23 µA from the external resistor divider.
3	2	7	OVP	Line Over-Voltage Protection	An external voltage divider from the power source sets the shutdown levels. The threshold is 1.25V. Hysteresis is set by an internal current source that sources 23µA into the external resistor divider.
4	3	8	COMP	Input to the Pulse Width Modulator	An external opto-coupler connected to the COMP pin sources current into an internal NPN current mirror. The PWM duty cycle is maximum with zero input current, while 1mA reduces the duty cycle to zero. The current mirror improves the frequency response by reducing the AC voltage across the opto-coupler detector.
5	4	9	RT	Oscillator Frequency Control and Sync Clock Input	Normally biased at 2V. An external resistor connected between RT and AGND sets the internal oscillator frequency. The internal oscillator can be synchronized to an external clock with a frequency higher than the free running frequency set by the RT resistor.
6	5	10	AGND	Analog Ground	Connect directly to Power Ground.
7	6	11	CS	Current Sense input for current limit	If CS exceeds 0.25V, the output pulse will be terminated, entering cycle-by-cycle current limit. An internal switch holds CS low for 50ns after HO or LO switches high to blank leading edge transients.
8	7	12	SS	Soft-start Input	An internal 110µA current source charges an external capacitor to set the soft-start rate. During a current limit restart sequence, the internal current source is reduced to 1.2µA to increase the delay before retry.
9	8	13	DLY	Timing programming pin for the LO and HO to SR1 and SR2 outputs.	An external resistor to ground sets the timing for the non-overlap time of HO to SR1 and LO to SR2.
10	9	14	RES	Restart Timer	If cycle-by-cycle current limit is exceeded during any cycle, a 22 µA current is sourced to the RES pin capacitor.If the RES capacitor voltage reaches 2.5V, the soft-start capacitor will be fully discharged and then released with a pull-up current of 1.2µA. After the first output pulse at LO (when SS >COMP offset, typically 1V), the SS pin charging current will revert to 110µA.

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Pin Descriptions for LM5035A and LM5035A–1 (continued)

HTSSOP 20 PIN LM5035A	WQFN PIN LM5035A	HTSSOP 28 PIN LM5035A-1	Name	Description	Application Information
11	11	15	HB	Boost voltage for the HO driver	An external diode is required from VCC to HB and an external capacitor is required from HS to HB to power the HO gate driver.
12	12	16	HS	Switch node	Connection common to the transformer and both power switches. Provides a return path for the HO gate driver.
13	13	17	HO	High side gate drive output.	Output of the high side PWM gate driver. Capable of sinking 2A peak current
14	14	19	LO	Low side gate dfrive output.	Output of the low side PWM gate driver. Capable of sinking 2A peak current.
15	15	20	PGND	Power Ground	Connect directly to Analog Ground.
16	16	21	VCC	Output of the high voltage start-up regulator.The VCC voltage is regulated to 7.6V.	If an auxiliary winding raises the voltage on this pin above the regulation setpoint, the Start-up Regulator will shutdown, thus reducing the internal power dissipation.
17	17	22	SR2	Synchronous rectifier driver output.	Control output of the synchronous FET gate. Capable of 0.5A peak current.
18	18	23	SR1	Synchronous rectifier driver output.	Control output of the synchronous FET gate. Capable of 0.5A peak current.
19	19	24	REF	Output of 5V Reference	Maximum output current is 20mA. Locally decoupled with a 0.1µF capacitor.
20	21	28	VIN	Input voltage source	Input to the Start-up Regulator. Operating input range is 13V to 100V with transient capability to 105V. For power sources outside of this range, the LM5035A can be biased directly at VCC by an external regulator.
		1	NC		
		2	NC		
		3	NC		
		4	NC		
		18	NC		
		25	NC		
		26	NC		
		27	NC		
EP	EP		EP	Exposed Pad, underside of package	No electrical contact. Connect to system ground plane for reduced thermal resistance.
	1		NC	No connection	No electrical contact.
	10		NC	No connection	No electrical contact.
	20		NC	No connection	No electrical contact.
	22		NC	No connection	No electrical contact.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings[1][2]

VIN to GND		-0.3V to 105V
HS to GND		-1V to 105V
HB to GND		-0.3V to 118V
HB to HS		-0.3V to 18V
VCC to GND		-0.3V to 16V
CS, RT, DLY to GND		-0.3V to 5.5V
COMP Input Current		10mA
All other inputs to GND		-0.3V to 7V
ESD Rating[3]	Human Body Model	2kV
Storage Temperature Range		-65°C to 150°C
Junction Temperature		150°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. 2kV for all pins except HB, HO and HS which are rated at 1.5kV.

Operating Ratings[1]

VIN Voltage	13V to 105V
External Voltage Applied to VCC	8V to 15V
Operating Junction Temperature	-40°C to +125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.

Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C, and those with **boldface** type apply over full **Operating Junction Temperature range**. V_{VIN} = 48V, V_{VCC} = 10V externally applied, R_{RT} = 15.0 kΩ, R_{DLY} = 27.4kΩ, V_{UVLO} = 3V, V_{OVP} = 0V unless otherwise stated. See [1] and [2].

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Startup Regulator (VCC pin)						
V_{VCC}	VCC voltage	I_{VCC} = 10mA	**7.3**	7.6	**7.9**	V
$I_{VCC(LIM)}$	VCC current limit	V_{VCC} = 7V	**25**	35		mA
V_{VCCUV}	VCC Under-voltage threshold (VCC increasing)	VIN = VCC, ΔV_{VCC} from the regulation setpoint	**0.2**	0.1		V
	VCC decreasing	VCC – PGND	**5.5**	6.2	**6.9**	V
I_{VIN}	Startup regulator current	VIN = 90V, UVLO = 0V		30	**70**	µA
	Supply current into VCC from external source	Outputs & COMP open, V_{VCC} = 10V, Outputs Switching		4	**6**	mA
Voltage Reference Regulator (REF pin)						
V_{REF}	REF Voltage	I_{REF} = 0mA	**4.85**	5	**5.15**	V
	REF Voltage Regulation	I_{REF} = 0 to 10mA		25	**50**	mV
	REF Current Limit	REF = 4.5V	**15**	20		mA
Under-Voltage Lock Out and shutdown (UVLO pin)						
V_{UVLO}	Under-voltage threshold		**1.212**	1.25	**1.288**	V
I_{UVLO}	Hysteresis current	UVLO pin sinking	**19**	23	**27**	µA
	Under-voltage Shutdown Threshold	UVLO voltage falling		0.3		V
	Under-voltage Standby Enable Threshold	UVLO voltage rising		0.4		V

(1) All limits are ensured. All electrical characteristics having room temperature limits are tested during production with T_A = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Typical specifications represent the most likely parametric norm at 25°C operation

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Electrical Characteristics (continued)

Specifications with standard typeface are for T_J = 25°C, and those with **boldface** type apply over full **Operating Junction Temperature range**. V_{VIN} = 48V, V_{VCC} = 10V externally applied, R_{RT} = 15.0 kΩ, R_{DLY} = 27.4kΩ, V_{UVLO} = 3V, V_{OVP} = 0V unless otherwise stated. See (1) and (2).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Over-Voltage Protection (OVP pin)						
V_{OVP}	Over-Voltage threshold		**1.212**	1.25	**1.288**	V
I_{OVP}	Hysteresis current	OVP pin sourcing	**19**	23	**27**	µA
Current Sense Input (CS Pin)						
V_{CS}	Current Limit Threshold		**0.228**	0.25	**0.272**	V
	CS delay to output	CS from zero to 1V. Time for HO and LO to fall to 90% of VCC. Output load = 0 pF.		80		ns
	Leading edge blanking time at CS			50		ns
	CS sink impedance (clocked)	Internal FET sink impedance		32	**60**	Ω
Current Limit Restart (RES Pin)						
V_{RES}	RES Threshold		**2.4**	2.5	**2.6**	V
	Charge source current	V_{RES} = 1.5V	**16**	22	**28**	µA
	Discharge sink current	V_{RES} = 1V	**8**	12	**16**	µA
Soft-Start (SS Pin)						
I_{SS}	Charging current in normal operation	V_{SS} = 0	**80**	110	**140**	µA
	Charging current during a hiccup mode restart	V_{SS} = 0	**0.6**	1.2	**1.8**	µA
	Soft-stop Current Sink	V_{SS} = 2.5V	**80**	110	**140**	µA
Oscillator (RT Pin)						
F_{SW1}	Frequency 1 (at HO, half oscillator frequency)	R_{RT} = 15 kΩ, T_J = 25°C	**185**	200	**215**	kHz
		R_{RT} = 15 kΩ, T_J = -40°C to 125°C	**180**		**220**	
F_{SW2}	Frequency 2 (at HO, half oscillator frequency)	R_{RT} = 5.49 kΩ	**430**	500	**570**	kHz
	DC level			2		V
	Input Sync threshold		**2.5**	3	**3.4**	V
PWM Controller (Comp Pin)						
	Delay to output			80		ns
V_{PWM-OS}	SS to RAMP offset		**0.7**	1	**1.2**	V
	Minimum duty cycle	SS = 0V			**0**	%
	Small signal impedance	I_{COMP} = 600µA, COMP current to PWM voltage		5000		Ω
Main Output Drivers (HO and LO Pins)						
	Output high voltage	I_{OUT} = 50mA, V_{HB} - V_{HO}, V_{VCC} - V_{LO}	**0.5**	0.25		V
	Output low voltage	I_{OUT} = 100 mA		0.2	**0.5**	V
	Rise time	C_{LOAD} = 1 nF		15		ns
	Fall time	C_{LOAD} = 1 nF		13		ns
	Deadtime, HO to LO, LO to HO	V_{DLY} = V_{REF}, I_{COMP} = 0mA	**45**	70	**100**	ns
	Peak source current	$V_{HO,LO}$ = 0V, V_{VCC} = 10V		1.25		A
	Peak sink current	$V_{HO,LO}$ = 10V, V_{VCC} = 10V		2		A
	HB Threshold	V_{CC} rising		3.8		V
Voltage Feed-Forward (RAMP Pin)						
	RAMP comparator threshold	COMP current = 0	**2.4**	2.5	**2.6**	V
Synchronous Rectifier Drivers (SR1, SR2)						
	Output high voltage	I_{OUT} = 10mA, V_{VCC} - V_{SR1}, V_{VCC} - V_{SR2}	**0.25**	0.1		V
	Output low voltage	I_{OUT} = 20 mA (sink)		0.08	**0.2**	V
	Rise time	C_{LOAD} = 1 nF		40		ns

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Electrical Characteristics (continued)

Specifications with standard typeface are for T_J = 25°C, and those with **boldface** type apply over full **Operating Junction Temperature range**. V_{VIN} = 48V, V_{VCC} = 10V externally applied, R_{RT} = 15.0 kΩ, R_{DLY} = 27.4kΩ, V_{UVLO} = 3V, V_{OVP} = 0V unless otherwise stated. See (1) and (2).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Fall time	C_{LOAD} = 1 nF		20		ns
	Peak source current	V_{SR} = 0, V_{VCC} = 10V		0.5		A
	Peak sink current	V_{SR} = V_{VCC}, V_{VCC} = 10V		0.5		A
T1	Deadtime, SR1 falling to HO rising, SR2 falling to LO rising	R_{DLY} = 10k		33		ns
		R_{DLY} = 27.4k	**68**	86	**120**	ns
		R_{DLY} = 100k		300		ns
T2	Deadtime, HO falling to SR1 rising, LO falling to SR2 rising	R_{DLY} = 10k		18		ns
		R_{DLY} = 27.4k	**20**	29	**42**	ns
		R_{DLY} = 100k		80		ns
Thermal Shutdown						
T_{SD}	Shutdown temperature			165		°C
	Hysteresis			20		°C
Thermal Resistance						
θ_{JA}	Junction to ambient, 0 LFPM Air Flow	HTSSOP-20 package		40		°C/W
θ_{JC}	Junction to Case (EP) Thermal resistance	HTSSOP-20 package		4		°C/W
θ_{JA}	Junction to ambient, 0 LFM Air Flow	WQFN-24 (4 mm x 5 mm)		40		°C/W
θ_{JC}	Junction to Case Thermal resistance	WQFN-24 (4 mm x 5 mm)		6		°C/W

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Typical Performance Characteristics

V_{VCC} and V_{REF} vs V_{VIN}

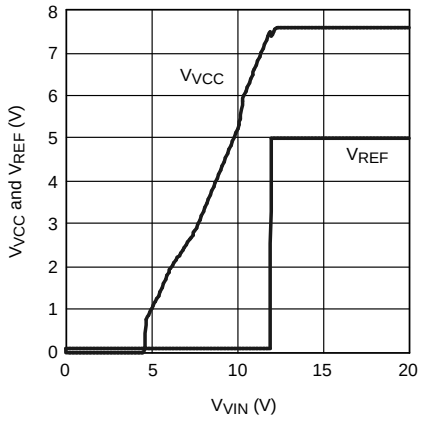


Figure 4.

V_{VCC} vs I_{VCC}

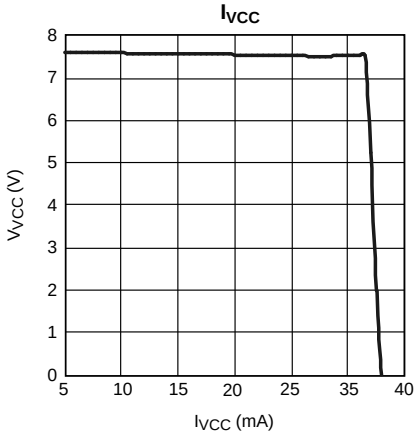


Figure 5.

V_{REF} vs I_{REF}

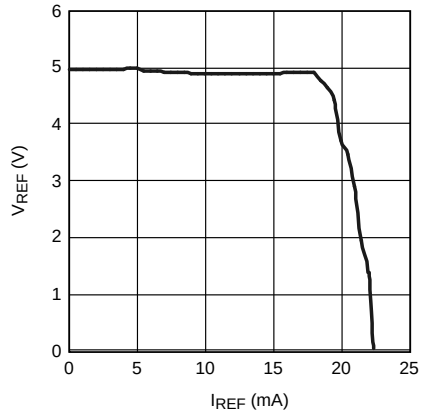


Figure 6.

Frequency vs RT

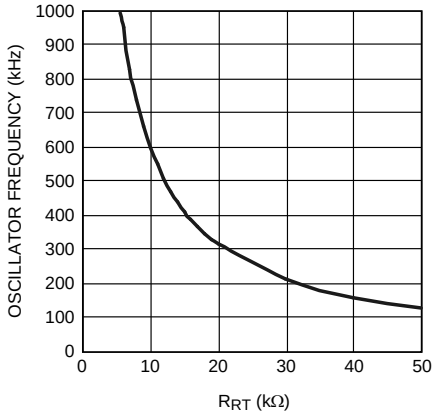


Figure 7.

Oscillator Frequency vs Temperature

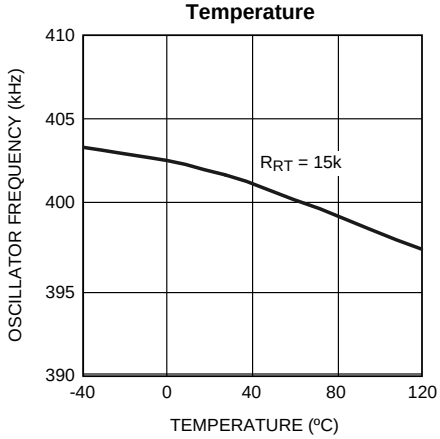


Figure 8.

Soft-Start & Stop Current vs Temperature

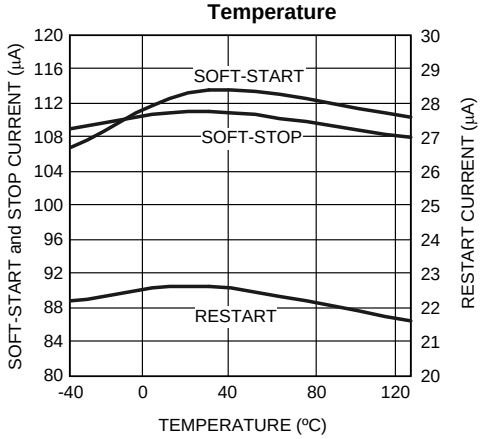


Figure 9.

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Typical Performance Characteristics (continued)

Effective Comp Input Impedance

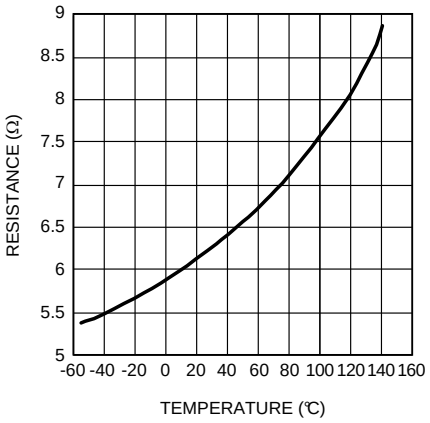


Figure 10.

R_{DLY} vs Deadtime

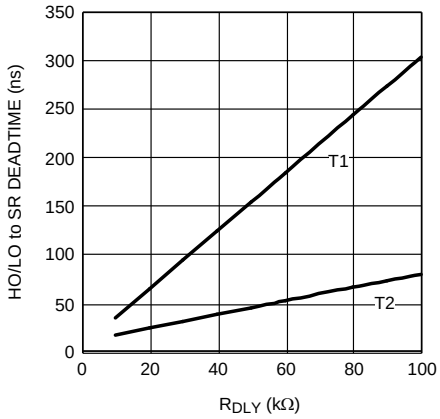


Figure 11.

SR "T1" Parameter vs Temperature

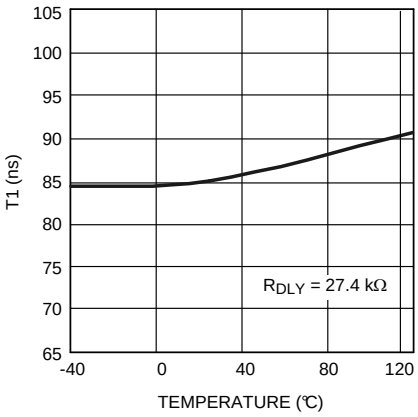


Figure 12.

SR "T2" Parameter vs Temperature

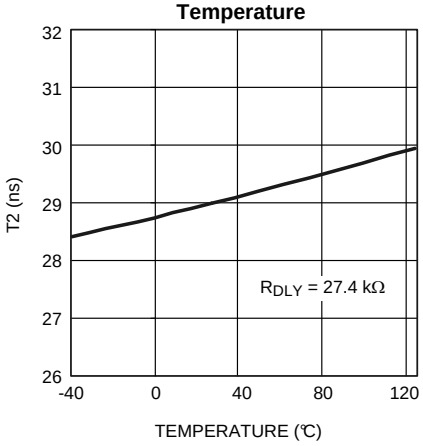
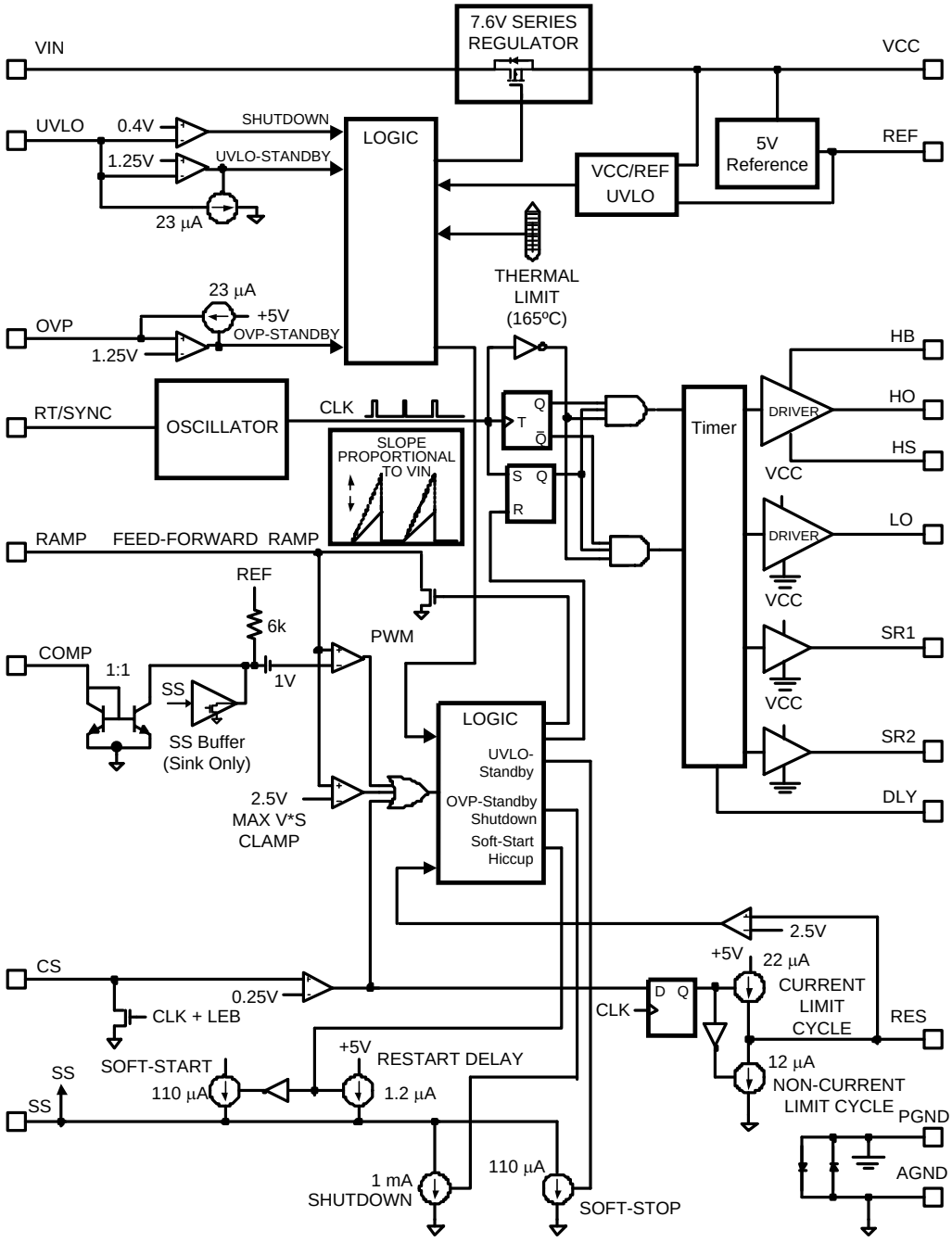


Figure 13.

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Block Diagram



FUNCTIONAL DESCRIPTION

The LM5035A PWM controller contains all of the features necessary to implement half-bridge voltage-mode controlled power converters. The LM5035A provides two gate driver outputs to directly drive the primary side power MOSFETs and two signal level outputs to control secondary synchronous rectifiers through an isolation interface. Secondary side drivers, such as the LM5110, are typically used to provide the necessary gate drive current to control the sync MOSFETs. Synchronous rectification allows higher conversion efficiency and greater power density than conventional PN or Schottky rectifier techniques. The LM5035A can be configured to operate with bias voltages ranging from 8V to 105V. Additional features include line under-voltage lockout, cycle-by-cycle current limit, voltage feed-forward compensation, hiccup mode fault protection with adjustable delays, soft-start, a 2MHz capable oscillator with synchronization capability, precision reference, thermal shutdown and programmable volt•second clamping. These features simplify the design of voltage-mode half-bridge DC-DC power converters. The Functional Block Diagram is shown in Block Diagram.

High-Voltage Start-up Regulator

The LM5035A contains an internal high voltage start-up regulator that allows the input pin (VIN) to be connected directly to a nominal 48 VDC input voltage. The regulator input can withstand transients up to 105V. The regulator output at VCC (7.6V) is internally current limited to 35 mA typical. When the UVLO pin potential is greater than 0.4V, the VCC regulator is enabled to charge an external capacitor connected to the VCC pin. The VCC regulator provides power to the voltage reference (REF) and the output drivers (LO, SR1 and SR2). When the voltage on the VCC pin exceeds the UVLO threshold of 7.6V, the internal voltage reference (REF) reaches its regulation setpoint of 5V and the UVLO voltage is greater than 1.25V, the controller outputs are enabled. The value of the VCC capacitor depends on the total system design, and its start-up characteristics. The recommended range of values for the VCC capacitor is 0.1 µF to 100 µF.

The VCC under-voltage comparator threshold is lowered to 6.2V (typical) after VCC reaches the regulation set-point. If VCC falls below this value, the outputs are disabled, and the soft-start capacitor is discharged. If VCC increases above 7.6V, the outputs will be enabled and a soft-start sequence will commence.

The internal power dissipation of the LM5035A can be reduced by powering VCC from an external supply. In typical applications, an auxiliary transformer winding is connected through a diode to the VCC pin. This winding must raise the VCC voltage above 8.3V to shut off the internal start-up regulator. Powering VCC from an auxiliary winding improves efficiency while reducing the controller's power dissipation. The under-voltage comparator circuit will still function in this mode, requiring that VCC never falls below 6.2V during the start-up sequence.

During a fault mode, when the converter auxiliary winding is inactive, external current draw on the VCC line should be limited such that the power dissipated in the start-up regulator does not exceed the maximum power dissipation of the IC package.

An external DC bias voltage can be used instead of the internal regulator by connecting the external bias voltage to both the VCC and the VIN pins. The external bias must be greater than 8.3V to exceed the VCC UVLO threshold and less than the VCC maximum operating voltage rating (15V).

Line Under-Voltage Detector

The LM5035A contains a dual level Under-Voltage Lockout (UVLO) circuit. When the UVLO pin voltage is below 0.4V, the controller is in a low current shutdown mode. When the UVLO pin voltage is greater than 0.4V but less than 1.25V, the controller is in standby mode. In standby mode the VCC and REF bias regulators are active while the controller outputs are disabled. When the VCC and REF outputs exceed the VCC and REF under-voltage thresholds and the UVLO pin voltage is greater than 1.25V, the outputs are enabled and normal operation begins. An external set-point voltage divider from VIN to GND can be used to set the minimum operating voltage of the converter. The divider must be designed such that the voltage at the UVLO pin will be greater than 1.25V when VIN enters the desired operating range. UVLO hysteresis is accomplished with an internal 23 µA current sink that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current sink is deactivated to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 1.25V threshold, the current sink is enabled causing the voltage at the UVLO pin to quickly fall. The hysteresis of the 0.4V shutdown comparator is internally fixed at 100 mV.

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The UVLO pin can also be used to implement various remote enable / disable functions. Turning off a converter by forcing the UVLO pin to the standby condition provides a controlled soft-stop. See the Soft-Start section for more details.

Line Over Voltage / Load Over Voltage / Remote Thermal Protection

The LM5035A provides a multipurpose OVP pin that supports several fault protection functions. When the OVP pin voltage exceeds 1.25V, the controller is held in standby mode which immediately halts the PWM pulses at the HO and LO pins. In standby mode, the VCC and REF bias regulators are active while the controller outputs are disabled. When the OVP pin voltage falls below the 1.25V OVP threshold, the outputs are enabled and normal soft-start sequence begins. Hysteresis is accomplished with an internal 23 µA current source that is switched on or off into the impedance of the OVP pin set-point divider. When the OVP threshold is exceeded, the current source is enabled to quickly raise the voltage at the OVP pin. When the OVP pin voltage falls below the 1.25V threshold, the current source is disabled causing the voltage at the OVP pin to quickly fall.

Several examples of the use of this pin are provided in the Application Information section.

Reference

The REF pin is the output of a 5V linear regulator that can be used to bias an opto-coupler transistor and external housekeeping circuits. The regulator output is internally current limited to 20mA (typical).

Cycle-by-Cycle Current Limit

The CS pin is driven by a signal representative of the transformer primary current. If the voltage sensed at CS pin exceeds 0.25V, the current sense comparator terminates the HO or LO output driver pulse. If the high current condition persists, the controller operates in a cycle-by-cycle current limit mode with duty cycle determined by the current sense comparator instead of the PWM comparator. Cycle-by-cycle current limiting may trigger the hiccup mode restart cycle depending on the configuration of the RES pin (see below).

A small R-C filter connect to the CS pin and located near the controller is recommended to suppress noise. An internal 32Ω MOSFET connected to the CS input discharges the external current sense filter capacitor at the conclusion of every cycle. The discharge MOSFET remains on for an additional 50 ns after the HO or LO driver switches high to blank leading edge transients in the current sensing circuit. Discharging the CS pin filter each cycle and blanking leading edge spikes reduces the filtering requirements and improves the current sense response time.

The current sense comparator is very fast and responds to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be placed very close to the device and connected directly to the CS and AGND pins. If a current sense transformer is used, both leads of the transformer secondary should be routed to the filter network, which should be located close to the IC. If a sense resistor located in the source of the main MOSFET switch is used for current sensing, a low inductance type of resistor is required. When designing with a current sense resistor, all of the noise sensitive low power ground connections should be connected together near the AGND pin, and a single connection should be made to the power ground (sense resistor ground point).

Overload Protection Timer

The LM5035A provides a current limit restart timer to disable the outputs and force a delayed restart (hiccup mode) if a current limit condition is repeatedly sensed. The number of cycle-by-cycle current limit events required to trigger the restart is programmable by the external capacitor at the RES pin. During each PWM cycle, the LM5035A either sources or sinks current from the RES pin capacitor. If no current limit is detected during a cycle, an 12 µA discharge current sink is enabled to pull the RES pin to ground. If a current limit is detected, the 12 µA sink current is disabled and a 22µA current source causes the voltage at the RES pin to gradually increase. The LM5035A protects the converter with cycle-by-cycle current limiting while the voltage at RES pin increases. If the RES voltage reaches the 2.5V threshold, the following restart sequence occurs (also see Figure 14):

- The RES capacitor and SS capacitors are fully discharged
- The soft-start current source is reduced from 110 µA to 1 µA
- The SS capacitor voltage slowly increases. When the SS voltage reaches ≅1V, the PWM comparator will produce the first narrow output pulse. After the first pulse occurs, the SS source current reverts to the normal 110 µA level. The SS voltage increases at its normal rate, gradually increasing the duty cycle of the output drivers

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- If the overload condition persists after restart, cycle-by-cycle current limiting will begin to increase the voltage on the RES capacitor again, repeating the hiccup mode sequence
- If the overload condition no longer exists after restart, the RES pin will be held at ground by the 12 µA current sink and normal operation resumes

The overload timer function is very versatile and can be configured for the following modes of protection:

1. **Cycle-by-cycle only**: The hiccup mode can be completely disabled by connecting a zero to 50 kΩ resistor from the RES pin to AGND. In this configuration, the cycle-by-cycle protection will limit the output current indefinitely and no hiccup sequences will occur.
2. **Hiccup only:** The timer can be configured for immediate activation of a hiccup sequence upon detection of an overload by leaving the RES pin open circuit.
3. **Delayed Hiccup:** Connecting a capacitor to the RES pin provides a programmed interval of cycle-by-cycle limiting before initiating a hiccup mode restart, as previously described. The dual advantages of this configuration are that a short term overload will not cause a hiccup mode restart but during extended overload conditions, the average dissipation of the power converter will be very low.
4. **Externally Controlled Hiccup:** The RES pin can also be used as an input. By externally driving the pin to a level greater than the 2.5V hiccup threshold, the controller will be forced into the delayed restart sequence. For example, the external trigger for a delayed restart sequence could come from an over-temperature protection circuit or an output over-voltage sensor.

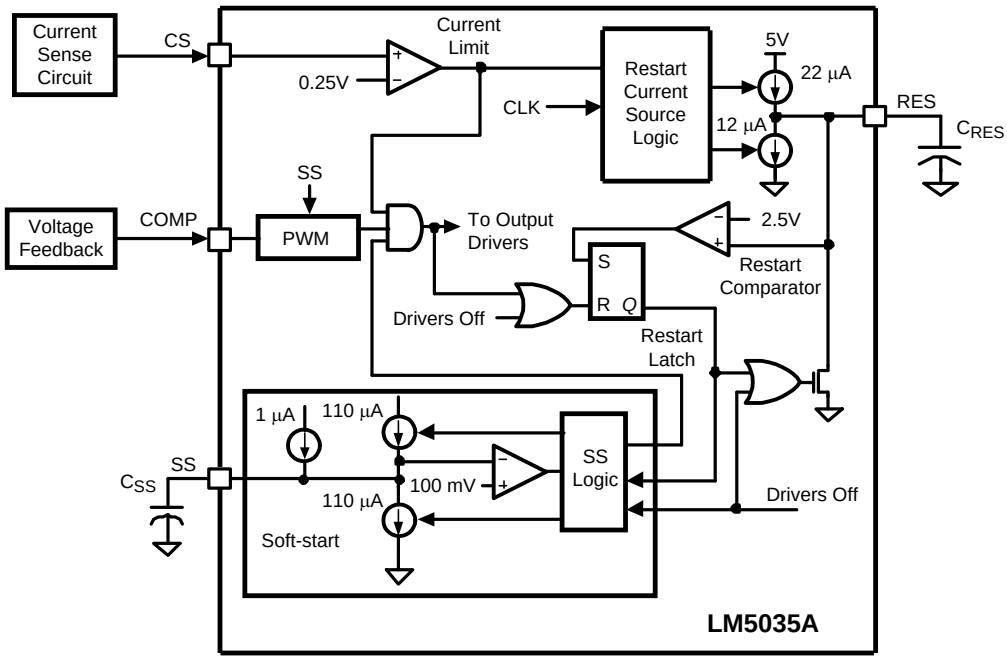


Figure 14. Current Limit Restart Circuit

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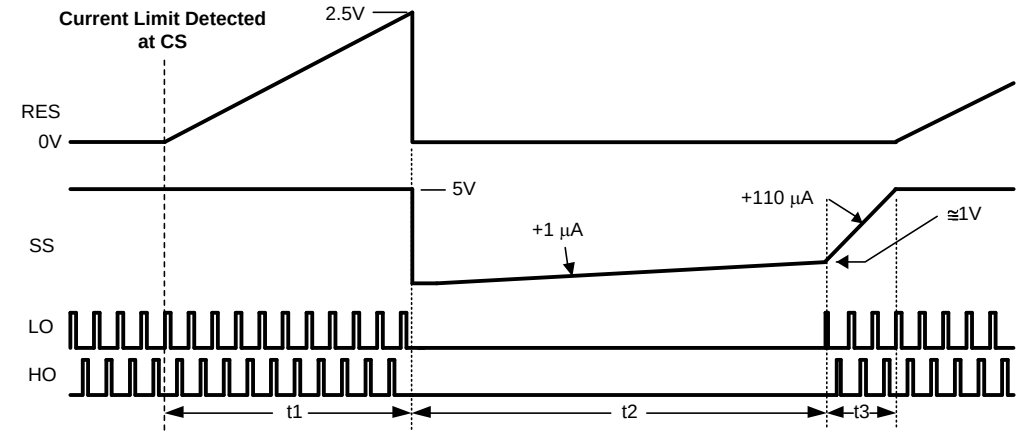


Figure 15. Current Limit Restart Timing

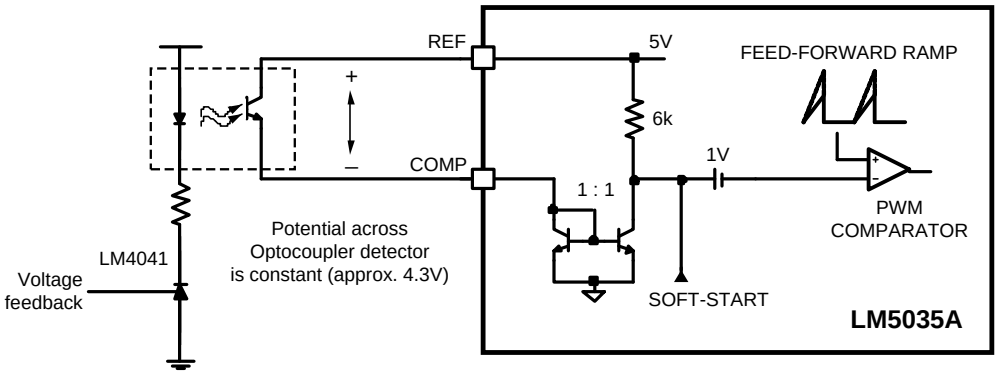


Figure 16. Optocoupler to COMP Interface

Soft-Start

The soft-start circuit allows the regulator to gradually reach a steady state operating point, thereby reducing start-up stresses and current surges. When bias is supplied to the LM5035A, the SS pin capacitor is discharged by an internal MOSFET. When the UVLO, VCC and REF pins reach their operating thresholds, the SS capacitor is released and charged with a 110 µA current source. The PWM comparator control voltage is clamped to the SS pin voltage by an internal amplifier. When the PWM comparator input reaches 1V, output pulses commence with slowly increasing duty cycle. The voltage at the SS pin eventually increases to 5V, while the voltage at the PWM comparator increases to the value required for regulation as determined by the voltage feedback loop.

One method to shutdown the regulator is to ground the SS pin. This forces the internal PWM control signal to ground, reducing the output duty cycle quickly to zero. Releasing the SS pin begins a soft-start cycle and normal operation resumes. A second shutdown method is discussed in the UVLO section.

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Soft-Stop

If the UVLO pin voltage falls below the 1.25V standby threshold but above the 0.4V shutdown threshold, the 110 µA SS pin source current is disabled and a 110 µA sink current discharges the soft-start capacitor. As SS voltage falls and clamps the PWM comparator input, the PWM duty cycle will gradually fall to zero. The soft-stop feature produces a gradual reduction of the power converter output voltage. This soft-stop method of turning off the converter reduces energy in the output capacitor before control of the main and synchronous rectification MOSFETs is disabled. The PWM pulses may cease before the SS voltage reduces the duty cycle if the VCC or REF voltage drops below the respective under-voltage thresholds during the soft-stop process.

PWM Comparator

The pulse width modulation (PWM) comparator compares the voltage ramp signal at the RAMP pin to the loop error signal. This comparator is optimized for speed in order to achieve minimum controllable duty cycles. The loop error signal is received from the external feedback and isolation circuit is in the form of a control current into the COMP pin. The COMP pin current is internally mirrored by a matched pair of NPN transistors which sink current through a 5 kΩ resistor connected to the 5V reference. The resulting control voltage passes through a 1V level shift before being applied to the PWM comparator.

An opto-coupler detector can be connected between the REF pin and the COMP pin. Because the COMP pin is controlled by a current input, the potential difference across the optocoupler detector is nearly constant. The bandwidth limiting phase delay which is normally introduced by the significant capacitance of the opto-coupler is thereby greatly reduced. Higher loop bandwidths can be realized since the bandwidth-limiting pole associated with the opto-coupler is now at a much higher frequency. The PWM comparator polarity is configured such that with no current into the COMP pin, the controller produces the maximum duty cycle at the main gate driver outputs, HO and LO.

Feed-Forward Ramp and Volt • Second Clamp

An external resistor (R_{FF}) and capacitor (C_{FF}) connected to VIN, AGND, and the RAMP pin are required to create the PWM ramp signal. The slope of the signal at RAMP will vary in proportion to the input line voltage. This varying slope provides line feed-forward information necessary to improve line transient response with voltage mode control. The RAMP signal is compared to the error signal by the pulse width modulator comparator to control the duty cycle of the HO and LO outputs. With a constant error signal, the on-time (T_{ON}) varies inversely with the input voltage (VIN) to stabilize the Volt • Second product of the transformer primary signal. The power path gain of conventional voltage-mode pulse width modulators (oscillator generated ramp) varies directly with input voltage. The use of a line generated ramp (input voltage feed-forward) nearly eliminates this gain variation. As a result, the feedback loop is only required to make very small corrections for large changes in input voltage.

In addition to the PWM comparator, a Volt • Second Clamp comparator also monitors the RAMP pin. If the ramp amplitude exceeds the 2.5V threshold of the Volt • Second Clamp comparator, the on-time is terminated. The C_{FF} ramp capacitor is discharged by an internal 32Ω discharge MOSFET controlled by the V•S Clamp comparator. If the RAMP signal does not exceed 2.5V before the end of the clock period, then the internal clock will enable the discharge MOSFET to reset capacitor C_{FF}.

By proper selection of R_{FF} and C_{FF} values, the maximum on-time of HO and LO can be set to the desired duration. The on-time set by the Volt • Second Clamp varies inversely to the line voltage because the RAMP capacitor is charged by a resistor (R_{FF}) connected to VIN while the threshold of the clamp is a fixed voltage (2.5V). An example will illustrate the use of the Volt • Second Clamp comparator to achieve a 50% duty cycle limit at 200kHz with a 48V line input. A 50% duty cycle at a 200kHz requires a 2.5µs on-time. To achieve this maximum on-time clamp level:

$$R_{FF} \times C_{FF} = \frac{T_{ON} + 10\%}{\ln\left[\left(1 - \frac{2.5V}{VIN}\right)^{-1}\right]} = \frac{2.5\ \mu s + 0.25\ \mu s}{\ln\left[\left(1 - \frac{2.5V}{48V}\right)^{-1}\right]} = 51.4\ \mu s \quad (1)$$

The recommended capacitor value range for C_{FF} is 100 pF to 1000 pF. 470 pF is a standard value that can be paired with an 110 kΩ to approximate the desired 51.4µs time constant. If load transient response is slowed by the 10% margin, the R_{FF} value can be increased. The system signal-to-noise will be slightly decreased by increasing $R_{FF} \times C_{FF}$.

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Oscillator, Sync Capability

The LM5035A oscillator frequency is set by a single external resistor connected between the RT and AGND pins. To set a desired oscillator frequency, the necessary RT resistor is calculated from:

$$RT = \left(\frac{1}{F_{OSC}} - 110\ ns \right) \times 6.25 \times 10^{9} \quad (2)$$

For example, if the desired oscillator frequency is 400kHz (HO and LO each switching at 200 kHz) a 15 kΩ resistor would be the nearest standard one percent value.

Each output (HO, LO, SR1 and SR2) switches at half the oscillator frequency. The voltage at the RT pin is internally regulated to a nominal 2V. The RT resistor should be located as close as possible to the IC, and connected directly to the pins (RT and AGND). The tolerance of the external resistor, and the frequency tolerance indicated in the Electrical Characteristics, must be taken into account when determining the worst case frequency range.

The LM5035A can be synchronized to an external clock by applying a narrow pulse to the RT pin. The external clock must be at least 10% higher than the free-running oscillator frequency set by the RT resistor. If the external clock frequency is less than the RT resistor programmed frequency, the LM5035A will ignore the synchronizing pulses. The synchronization pulse width at the RT pin must be a minimum of 15 ns wide. The clock signal should be coupled into the RT pin through a 100 pF capacitor or a value small enough to ensure the pulse width at RT is less than 60% of the clock period under all conditions. When the synchronizing pulse transitions low-to-high (rising edge), the voltage at the RT pin must be driven to exceed 3.2V volts from its nominal 2 VDC level. During the clock signal's low time, the voltage at the RT pin will be clamped at 2 VDC by an internal regulator. The output impedance of the RT regulator is approximately 100Ω. The RT resistor is always required, whether the oscillator is free running or externally synchronized.

Gate Driver Outputs (HO & LO)

The LM5035A provides two alternating gate driver outputs, the floating high side gate driver HO and the ground referenced low side driver LO. Each driver is capable of sourcing 1.25A and sinking 2A peak. The HO and LO outputs operate in an alternating manner, at one-half the internal oscillator frequency. The LO driver is powered directly by the VCC regulator. The HO gate driver is powered from a bootstrap capacitor connected between HB and HS. An external diode connected between VCC (anode pin) and HB (cathode pin) provides the high side gate driver power by charging the bootstrap capacitor from VCC when the switch node (HS pin) is low. When the high side MOSFET is turned on, HB rises to a peak voltage equal to $V_{VCC} + V_{HS}$ where V_{HS} is the switch node voltage.

The HB and VCC capacitors should be placed close to the pins of the LM5035A to minimize voltage transients due to parasitic inductances since the peak current sourced to the MOSFET gates can exceed 1.25A. The recommended value of the HB capacitor is 0.01 µF or greater. A low ESR / ESL capacitor, such as a surface mount ceramic, should be used to prevent voltage droop during the HO transitions.

The maximum duty cycle for each output is limited to slightly less than 50% due to the internally fixed deadtime and any programmed sync rectifier delay. The typical deadtime in this condition is 70 ns. The programmed sync rectifier delay is determined by the DLY pin resistor. If the COMP pin is open circuit, the outputs will operate at maximum duty cycle. The maximum duty cycle for each output can be calculated with the following equation:

$$\text{Maximum Duty Cycle} = \frac{\frac{1}{2}T_S - T_D - T1}{T_S} \quad (3)$$

Where T_S is the period of one complete cycle for either the HO or LO outputs, TD is the internally fixed deadtime, and T1 is the programmed sync rectifier delay. For example, if the oscillator frequency is 200 kHz, each output will cycle at 100 kHz (T_S = 10 µs). Using the nominal deadtime of 70 ns and no programmed delay, the maximum duty cycle at this frequency is calculated to be 49.3%. Using a programmed sync rectifier delay of 100 ns, the maximum duty cycle is reduced to 48.3%.

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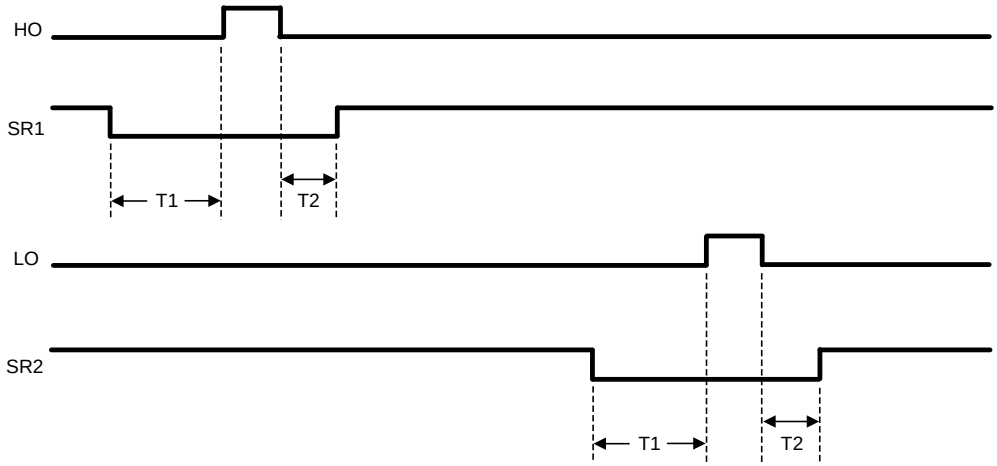


Figure 17. HO, LO, SR1 and SR2 Timing Diagram

Synchronous Rectifier Control Outputs (SR1 & SR2)

Synchronous rectification (SR) of the transformer secondary provides higher efficiency, especially for low output voltage converters. The reduction of rectifier forward voltage drop (0.5V - 1.5V) to 10mV - 200mV V_{DS} voltage for a MOSFET significantly reduces rectification losses. In a typical application, the transformer secondary winding is center tapped, with the output power inductor in series with the center tap. The SR MOSFETs provide the ground path for the energized secondary winding and the inductor current. Figure 17 shows that the SR2 MOSFET is conducting while HO enables power transfer from the primary. The SR1 MOSFET must be disabled during this period since the secondary winding connected to the SR1 MOSFET drain is twice the voltage of the center tap. At the conclusion of the HO pulse, the inductor current continues to flow through the SR1 MOSFET body diode. Since the body diode causes more loss than the SR MOSFET, efficiency can be improved by minimizing the T2 period while maintaining sufficient timing margin over all conditions (component tolerances, etc.) to prevent shoot-through current. When LO enables power transfer from the primary, the SR1 MOSFET is enabled and the SR2 MOSFET is off.

During the time that neither HO nor LO is active, the inductor current is shared between both the SR1 and SR2 MOSFETs which effectively shorts the transformer secondary and cancels the inductance in the windings. The SR2 MOSFET is disabled before LO delivers power to the secondary to prevent power being shunted to ground. The SR2 MOSFET body diode continues to carry about half the inductor current until the primary power raises the SR2 MOSFET drain voltage and reverse biases the body diode. Ideally, dead-time T1 would be set to the minimum time that allows the SR MOSFET to turn off before the SR MOSFET body diode starts conducting.

The SR1 and SR2 outputs are powered directly by the VCC regulator. Each output is capable of sourcing and sinking 0.5A peak. Typically, the SR1 and SR2 signals control SR MOSFET gate drivers through a pulse transformer. The actual gate sourcing and sinking currents are provided by the secondary-side bias supply and gate drivers.

The timing of SR1 and SR2 with respect to HO and LO is shown in Figure 17. SR1 is configured out of phase with HO and SR2 is configured out of phase with LO. The deadtime between transitions is programmable by a resistor connected from the DLY pin to the AGND pin. Typically, R_{DLY} is set in the range of 10kΩ to 100kΩ. The deadtime periods can be calculated using the following formulae:

$$T1 = .003 \times R_{DLY} + 4.6\ ns \quad (4)$$

$$T2 = .0007 \times R_{DLY} + 10.01\ ns \quad (5)$$

To set the minimum (propagation delays only) deadtime, the DLY pin should be left open or connected to the REF pin. Any resistor value above 300kΩ connected between the DLY pin and AGND will also provide the minimum period (approximately 5 ns).

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Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event the maximum rated junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power standby state with the output drivers (HO, LO, SR1 and SR2), the bias regulators (VCC and REF) disabled. This helps to prevent catastrophic failures from accidental device overheating. During thermal shutdown, the soft-start capacitor is fully discharged and the controller follows a normal start-up sequence after the junction temperature falls to the operating level (145°C).

Applications Information

The following information is intended to provide guidelines for the power supply designer using the LM5035A.

VIN

The voltage applied to the VIN pin, which may be the same as the system voltage applied to the power transformer's primary (V_{PWR}), can vary in the range of 13 to 105V. The current into VIN depends primarily on the gate charge provided to the output drivers, the switching frequency, and any external loads on the VCC and REF pins. It is recommended the filter shown in Figure 18 be used to suppress transients which may occur at the input supply. This is particularly important when VIN is operated close to the maximum operating rating of the LM5035A.

When power is applied to VIN and the UVLO pin voltage is greater than 0.4V, the VCC regulator is enabled and supplies current into an external capacitor connected to the VCC pin. When the voltage on the VCC pin reaches the regulation point of 7.6V, the voltage reference (REF) is enabled. The reference regulation set point is 5V. The HO, LO, SR1 and SR2 outputs are enabled when the two bias regulators reach their set point and the UVLO pin potential is greater than 1.25V. In typical applications, an auxiliary transformer winding is connected through a diode to the VCC pin. This winding must raise the VCC voltage above 8.3V to shut off the internal start-up regulator.

After the outputs are enabled and the external VCC supply voltage has begun supplying power to the IC, the current into VIN drops below 1 mA. VIN should remain at a voltage equal to or above the VCC voltage to avoid reverse current through protection diodes.

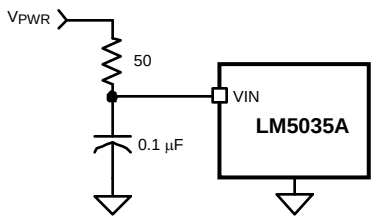


Figure 18. Input Transient Protection

FOR APPLICATIONS >100V

For applications where the system input voltage exceeds 100V or the IC power dissipation is of concern, the LM5035A can be powered from an external start-up regulator as shown in Figure 19. In this configuration, the VIN and the VCC pins should be connected together, which allows the LM5035A to be operated below 13V. The voltage at the VCC pin must be greater than 8.3V yet not exceed 15V. An auxiliary winding can be used to reduce the power dissipation in the external regulator once the power converter is active. The NPN base-emitter reverse breakdown voltage, which can be as low as 5V for some transistors, should be considered when selecting the transistor.

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CURRENT SENSE

The CS pin needs to receive an input signal representative of the transformer's primary current, either from a current sense transformer or from a resistor in series with the source of the LO switch, as shown in Figure 20 and Figure 21. In both cases, the sensed current creates a ramping voltage across R1, and the R_F/C_F filter suppresses noise and transients. R1, R_F and C_F should be located as close to the LM5035A as possible, and the ground connection from the current sense transformer, or R1, should be a dedicated track to the AGND pin. The current sense components must provide greater than 0.25V at the CS pin when an over-current condition exists.

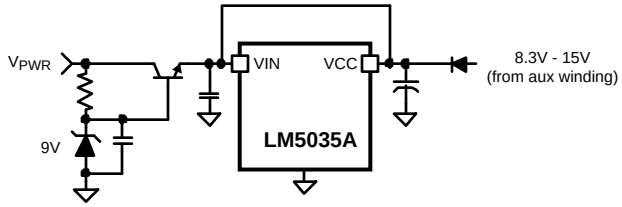


Figure 19. Start-up Regulator for V_{PWR} >100V

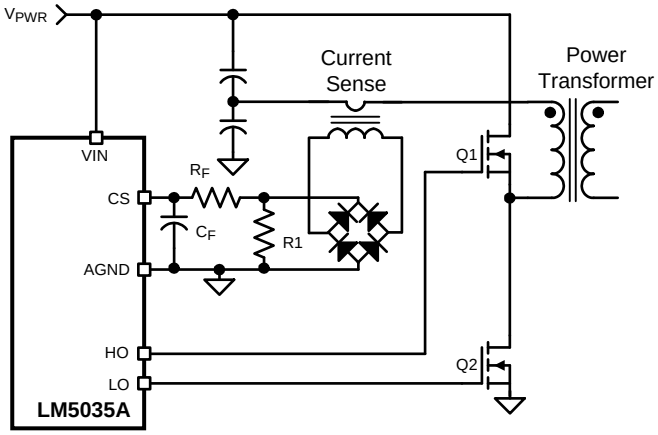


Figure 20. Current Sense Using Current Sense Transformer

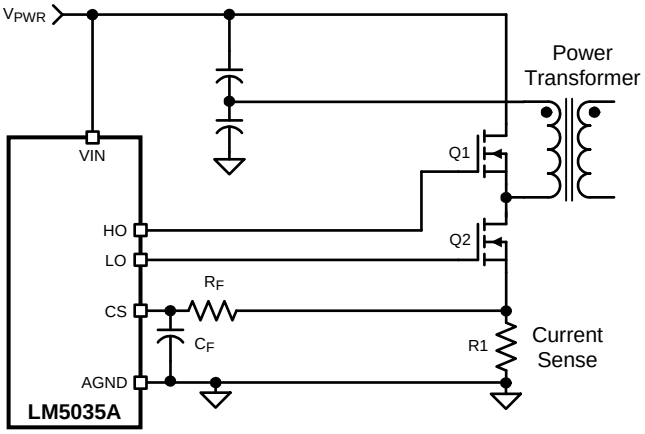


Figure 21. Current Sense Using Current Sense Resistor (R1)

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If the current sense resistor method is used, the over-current condition will only be sensed while LO is driving the low-side MOSFET. Over-current while HO is driving the high-side MOSFET will not be detected. In this configuration, it will take 4 times as long for continuous cycle-by-cycle current limiting to initiate a restart event since each over-current event during LO enables the 22µA RES pin current source for one oscillator period, and then the lack of an over-current event during HO enables the 12µA RES pin current sink for one oscillator period. The time average of this toggling is equivalent to a continuous 5 µA current source into the RES capacitor, increasing the delay by a factor of four. The value of the RES capacitor can be reduced to decrease the time before restart cycle is initiated.

When using the resistor current sense method, an imbalance in the input capacitor voltages may develop when operating in cycle-by-cycle current limiting mode. If the imbalance persists for an extended period, excessive currents in the non-sensed MOSFET, and possible transformer saturation may result. This condition is inherent to the half-bridge topology operated with cycle-by-cycle current limiting and is compounded by only sensing in one leg of the half-bridge circuit. The imbalance is greatest at large duty cycles (low input voltages). If using this method, it is recommended that the capacitor on the RES pin be no larger than 220 pF. Check the final circuit and reduce the RES capacitor further, or omit the capacitor completely to ensure the voltages across the bridge capacitors remain balanced. The current limit value may decrease slightly as the RES capacitor is reduced.

HO, HB, HS and LO

Attention must be given to the PC board layout for the low-side driver and the floating high-side driver pins HO, HB and HS. A low ESR/ESL capacitor (such as a ceramic surface mount capacitor) should be connected close to the LM5035A, between HB and HS to provide high peak currents during turn-on of the high-side MOSFET. The capacitor should be large enough to supply the MOSFET gate charge (Qg) without discharging to the point where the drop in gate voltage affects the MOSFET $R_{DS(ON)}$. A value ten to twenty times Qg is recommended.

$$C_{BOOST} = 20 \times \frac{Q_g}{VCC} \tag{6}$$

The diode (D_{BOOST}) that charges C_{BOOST} from VCC when the low-side MOSFET is conducting should be capable of withstanding the full converter input voltage range. When the high-side MOSFET is conducting, the reverse voltage at the diode is approximately the same as the MOSFET drain voltage because the high-side driver is boosted up to the converter input voltage by the HS pin, and the high side MOSFET gate is driven to the HS voltage plus VCC. Since the anode of D_{BOOST} is connected to VCC, the reverse potential across the diode is equal to the input voltage minus the VCC voltage. D_{BOOST} average current is less than 20mA in most applications, so a low current ultra-fast recovery diode is recommended to limit the loss due to diode junction capacitance. Schottky diodes are also a viable option, particularly for lower input voltage applications, but attention must be paid to leakage currents at high temperatures.

The internal gate drivers need a very low impedance path to the respective decoupling capacitors; the VCC cap for the LO driver and C_{BOOST} for the HO driver. These connections should be as short as possible to reduce inductance and as wide as possible to reduce resistance. The loop area, defined by the gate connection and its respective return path, should be minimized.

The high-side gate driver can also be used with HS connected to PGND for applications other than a half bridge converter (e.g. Push-Pull). The HB pin is then connected to VCC, or any supply greater than the high-side driver undervoltage lockout (approximately 6.5V). In addition, the high-side driver can be configured for high voltage offline applications where the high-side MOSFET gate is driven via a gate drive transformer.

PROGRAMMABLE DELAY (DLY)

The R_{DLY} resistor programs the delays between the SR1 and SR2 signals and the HO and LO driver outputs. Figure 17 shows the relationship between these outputs. The DLY pin is nominally set at 2.5V and the current is sensed through R_{DLY} to ground. This current is used to adjust the amount of deadtime before the HO and LO pulse (T1) and after the HO and LO pulse (T2). Typically R_{DLY} is in the range of 10kΩ to 100kΩ. The deadtime periods can be calculated using the following formulae:

$$T1 = .003 \times R_{DLY} + 4.6 \text{ ns} \tag{7}$$

$$T2 = .0007 \times R_{DLY} + 10.01 \text{ ns} \tag{8}$$

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T1 and T2 can be set to minimum by not connecting a resistor to DLY, connecting a resistor greater than 300kΩ from DLY to ground, or connecting DLY to the REF pin. This may cause lower than optimal system efficiency if the delays through the SR signal transformer network, the secondary gate drivers and the SR MOSFETs are greater than the delay to turn on the HO or LO MOSFETs. Should an SR MOSFET remain on while the opposing primary MOSFET is supplying power through the power transformer, the secondary winding will experience a momentary short circuit, causing a significant power loss to occur.

When choosing the R_{DLY} value, worst case propagation delays and component tolerances should be considered to assure that there is never a time where both SR MOSFETs are enabled AND one of the primary side MOSFETs is enabled. The time period T1 should be set so that the SR MOSFET has turned off before the primary MOSFET is enabled. Conversely, T1 and T2 should be kept as low as tolerances allow to optimize efficiency. The SR body diode conducts during the time between the SR MOSFET turns off and the power transformer begins supplying energy. Power losses increase when this happens since the body diode voltage drop is many times higher than the MOSFET channel voltage drop. The interval of body diode conduction can be observed with an oscilloscope as a negative 0.7V to 1.5V pulse at the SR MOSFET drain.

UVLO AND OVP VOLTAGE DIVIDER SELECTION FOR R1, R2, AND R3

Two dedicated comparators connected to the UVLO and OVP pins are used to detect under-voltage and over-voltage conditions. The threshold value of these comparators, V_{UVLO} and V_{OVP}, is 1.25V (typical). The two functions can be programmed independently with two voltage dividers from VIN to AGND as shown in Figure 22 and Figure 23, or with a three-resistor divider as shown in Figure 24. Independent UVLO and OVP pins provide greater flexibility for the user to select the operational voltage range of the system. Hysteresis is accomplished by 23 µA current sources (I_{UVLO} and I_{OVP}), which are switched on or off into the sense pin resistor dividers as the comparators change state.

When the UVLO pin voltage is below 0.4V, the controller is in a low current shutdown mode. For a UVLO pin voltage greater than 0.4V but less than 1.25V the controller is in standby mode. Once the UVLO pin voltage is greater than 1.25V, the controller is fully enabled. Two external resistors can be used to program the minimum operational voltage for the power converter as shown in Figure 22. When the UVLO pin voltage falls below the 1.25V threshold, an internal 23 µA current sink is enabled to lower the voltage at the UVLO pin, thus providing threshold hysteresis. Resistance values for R1 and R2 can be determined from the following equations.

$$R_1 = \frac{V_{HYS}}{23\ \mu A} \tag{9}$$

$$R_2 = \frac{1.25V \times R_1}{V_{PWR} - 1.25V - (23\ \mu A \times R_1)} \tag{10}$$

where V_{PWR} is the desired turn-on voltage and V_{HYS} is the desired UVLO hysteresis at V_{PWR}.

For example, if the LM5035A is to be enabled when V_{PWR} reaches 34V, and disabled when VPWR is decreased to 32V, R1 should be 87 kΩ, and R2 should be 3.54kΩ. The voltage at the UVLO pin should not exceed 7V at any time. Be sure to check both the power and voltage rating (0603 resistors can be rated as low as 50V) for the selected R1 resistor.

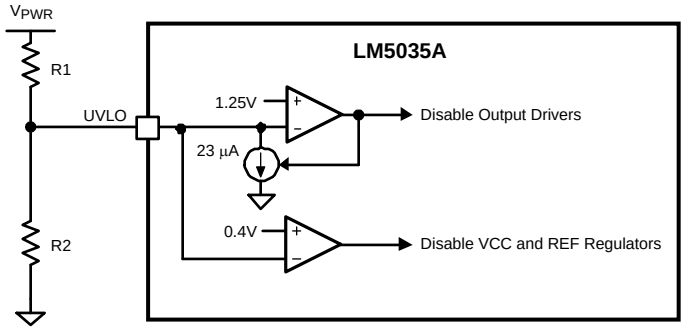


Figure 22. Basic UVLO Configuration

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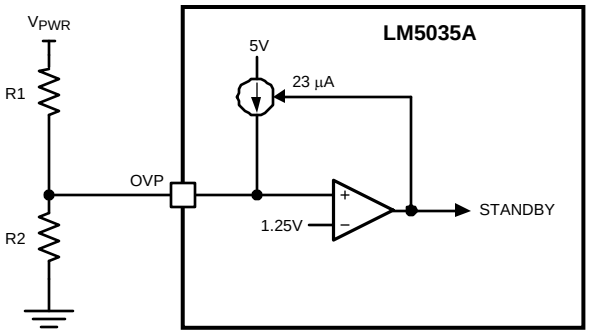


Figure 23. Basic Over-Voltage Protection

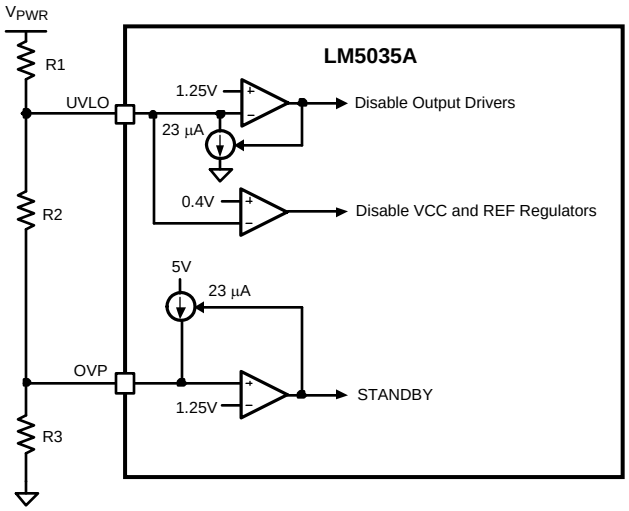


Figure 24. UVLO/OVP Divider

The impedance seen looking into the resistor divider from the UVLO and OVP pins determines the hysteresis level. UVLO and OVP enable and disable thresholds are calculated using the equations in the table below for the three-resistor divider illustrated in Figure 24.

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Table 1. UVO/OVP Divider Formulas

Outputs disabled due to VIN falling below UVLO threshold	$UVLO_{off} = 1.25V \times \left(\frac{R_1 + R_2 + R_3}{R_2 + R_3}\right)$ (11)
Outputs enabled due to VIN rising above UVLO threshold	$UVLO_{on} = UVLO_{off} + (23\ \mu A \times R_1)$
Outputs disabled due to VIN rising above OVP threshold	$OVP_{off} = 1.25V \times \left(\frac{R_1 + R_2 + R_3}{R_3}\right)$ (12)
Outputs enabled due to VIN falling below OVP threshold	$OVP_{on} = OVP_{off} - [23\ \mu A \times (R1 + R2)]$

The typical operating ranges of undervoltage and overvoltage thresholds are calculated from the above equations. For example, for resistor values R1 = 86.6kΩ, R2 = 2.10kΩ and R3 = 1.40kΩ the computed thresholds are:

UVLO turn-off = 32.2V

UVLO turn-on = 34.2V

OVP turn-on = 78.4V

OVP turn-off = 80.5V

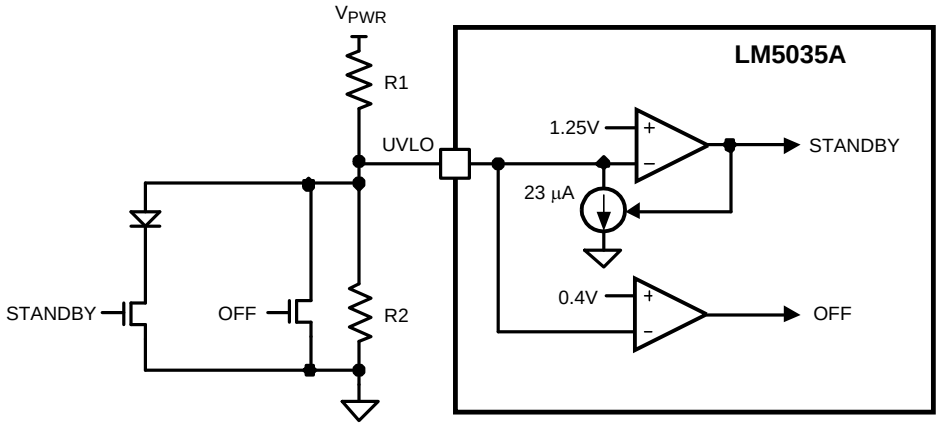


Figure 25. Remote Standby and Disable Control

To maintain the threshold's accuracy, a resistor tolerance of 1% or better is recommended.

The design process starts with the choice of the voltage difference between the UVLO enabling and disabling thresholds. This will also approximately set the difference between OVP enabling and disabling regulation:

$$R_1 = \frac{UVLO_{on} - UVLO_{off}}{23\ \mu A} \quad (13)$$

Next, the combined resistance of R_2 and R_3 is calculated by choosing the threshold for the UVLO disabling threshold:

$$R_{COMBINED} = \frac{1.25V \times R_1}{UVLO_{off} - 1.25V} \quad (14)$$

Then R_3 is determined by selecting the OVP disabling threshold:

$$R_3 = \frac{1.25V \times (R_1 + R_{COMBINED})}{OVP_{off}} \quad (15)$$

Finally, R_3 is subtracted from $R_{COMBINED}$ to give R_2:

$$\mathbf{R_2 = R_{COMBINED} - R_3} \quad (16)$$

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Remote configuration of the controller's operational modes can be accomplished with open drain device(s) connected to the UVLO pin as shown in Figure 25.

FAULT PROTECTION

The Over Voltage Protection (OVP) comparator of the LM5035A can be configured for line or load fault protection or thermal protection using an external temperature sensor or thermistor. Figure 23 shows a line over voltage shutdown application using a voltage divider between the input power supply, V_{PWR}, and AGND to monitor the line voltage.

Figure 26 demonstrates the use of the OVP pin for latched output over-voltage fault protection, using a zener and opto-coupler. When V_{OUT} exceeds the conduction threshold of the opto-coupler diode and zener, the opto-coupler momentarily turns on Q1 and the LM5035A enters standby mode, disabling the drivers and enabling the hysteresis current source on the OVP pin. Once the current source is enabled, the OVP voltage will remain at 2.3V (23 µA x 100 kΩ) without additional drive from the external circuit. If the opto-coupler transistor emitter were directly connected to the OVP pin, then leakage current in the zener diode amplified by the opto-coupler's gain could falsely trip the protection latch. R1 and Q1 are added reduce the sensitivity to low level currents in the opto-coupler. Using the values of Figure 26, the opto-coupler collector current must equal $V_{BE(Q1)}$ / R1 = 350 µA before OVP latches. Once the controller has switched to standby mode, the outputs no longer switch but the VCC and REF regulators continue functioning and supply bias to the external circuitry. VCC must fall below 6.2V or the UVLO pin must fall below 0.4V to clear the OVP latch.

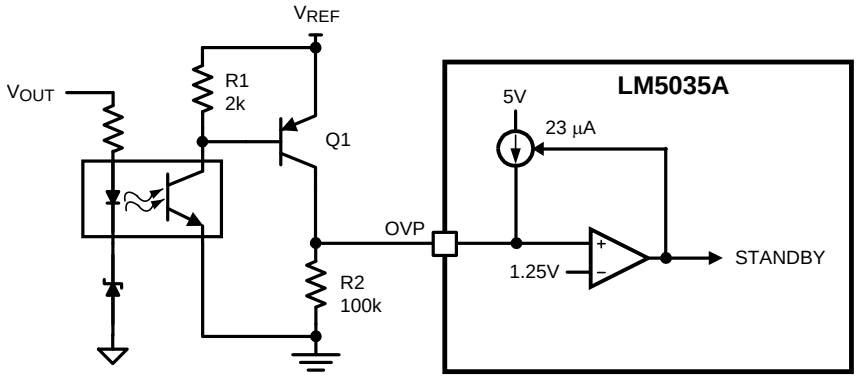


Figure 26. Latched Load Over-Voltage Protection

Figure 27 shows an application of the OVP comparator for Remote Thermal Protection using a thermistor (or multiple thermistors) which may be located near the main heat sources of the power supply. The negative temperature coefficient (NTC) thermistor is nearly logarithmic, and in this example a 100kΩ thermistor with the β material constant of 4500 kelvins changes to approximately 2 kΩ at 130°C. Setting R1 to one-third of this resistance (665Ω) establishes 130°C as the desired trip point (for V_{REF} = 5V). In a temperature band from 20°C below to 20°C above the OVP threshold, the voltage divider is nearly linear with 25 mV per°C sensitivity.

R2 provides temperature hysteresis by raising the OVP comparator input by R2 x 23 µA. For example, if a 22kΩ resistor is selected for R2, then the OVP pin voltage will increase by 22 kΩ x 23 µA = 506 mV. The NTC temperature must therefore fall by 506mV / 25mV per°C = 20°C before the LM5035A switches from the standby mode to the normal mode.

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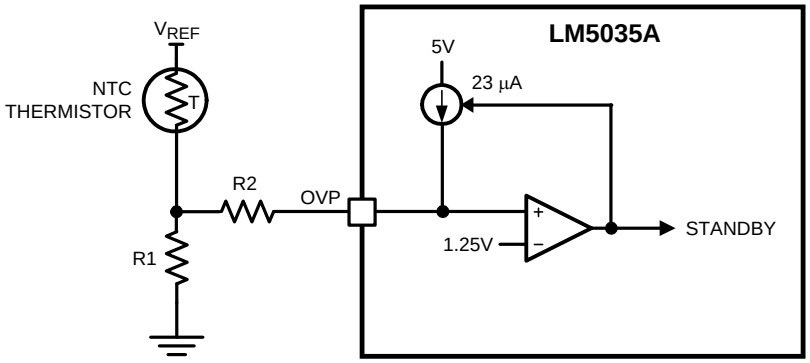


Figure 27. Remote Thermal Protection

HICCUP MODE CURRENT LIMIT RESTART (RES)

The basic operation of the hiccup mode current limit restart is described in the functional description. The delay time to restart is programmed with the selection of the RES pin capacitor C_{RES} as illustrated in Figure 27.

In the case of continuous cycle-by-cycle current limit detection at the CS pin, the time required for C_{RES} to reach the 2.5V hiccup mode threshold is:

$$t1 = \frac{C_{RES} \times 2.5V}{22\ \mu A} = 114\ k\Omega \times C_{RES} \tag{17}$$

For example, if C_{RES} = 0.01 µF the time t1 is approximately 1.14 ms.

The cool down time, t2 is set by the soft-start capacitor (C_{SS}) and the internal 1 µA SS current source, and is equal to:

$$t2 = \frac{C_{SS} \times 1V}{1\ \mu A} = 1\ M\Omega \times C_{SS} \tag{18}$$

If C_{SS} = 0.01 µF t2 is ≅10 ms.

The soft-start time t3 is set by the internal 110 µA current source, and is equal to:

$$t3 = \frac{C_{SS} \times 4V}{110\ \mu A} = 40\ k\Omega \times C_{SS} \tag{19}$$

If C_{SS} = 0.01 µF t3 is ≅363 µs.

The time t2 provides a periodic cool-down time for the power converter in the event of a sustained overload or short circuit. This off time results in lower average input current and lower power dissipation within the power components. It is recommended that the ratio of t2 / (t1 + t3) be in the range of 5 to 10 to take advantage of this feature.

If the application requires no delay from the first detection of a current limit condition to the onset of the hiccup mode (t1 = 0), the RES pin can be left open (no external capacitor). If it is desired to disable the hiccup mode entirely, the RES pin should be connected to ground (AGND).

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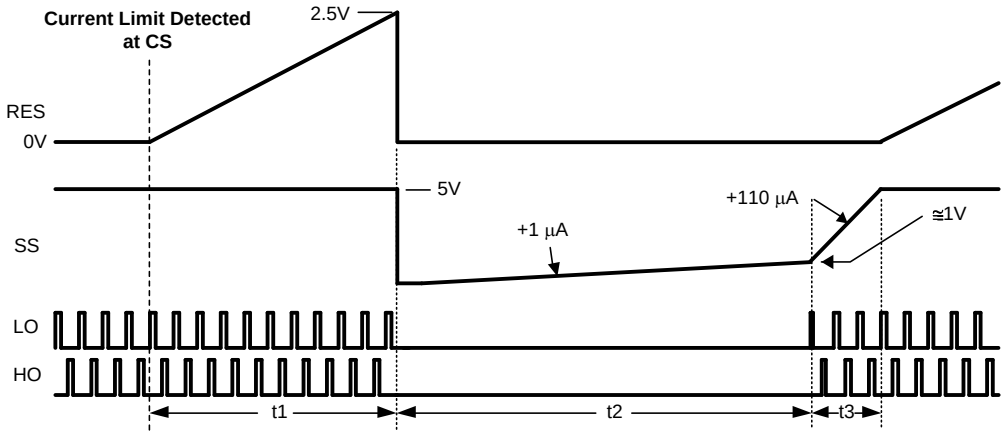


Figure 28. Hiccup Over-Load Restart Timing

Printed Circuit Board Layout

The LM5035A Current Sense and PWM comparators are very fast, and respond to short duration noise pulses. The components at the CS, COMP, SS, OVP, UVLO, DLY and the RT pins should be as physically close as possible to the IC, thereby minimizing noise pickup on the PC board tracks.

Layout considerations are critical for the current sense filter. If a current sense transformer is used, both leads of the transformer secondary should be routed to the sense filter components and to the IC pins. The ground side of the transformer should be connected via a dedicated PC board track to the AGND pin, rather than through the ground plane.

If the current sense circuit employs a sense resistor in the drive transistor source, low inductance resistors should be used. In this case, all the noise sensitive, low-current ground tracks should be connected in common near the IC, and then a single connection made to the power ground (sense resistor ground point).

The gate drive outputs of the LM5035A should have short, direct paths to the power MOSFETs in order to minimize inductance in the PC board traces. The SR control outputs should also have minimum routing distance through the pulse transformers and through the secondary gate drivers to the sync FETs.

The two ground pins (AGND, PGND) must be connected together with a short, direct connection, to avoid jitter due to relative ground bounce.

If the internal dissipation of the LM5035A produces high junction temperatures during normal operation, the use of multiple vias under the IC to a ground plane can help conduct heat away from the IC. Judicious positioning of the PC board within the end product, along with use of any available air flow (forced or natural convection) will help reduce the junction temperatures. If using forced air cooling, avoid placing the LM5035A in the airflow shadow of tall components, such as input capacitors.

Application Circuit Example

The following schematic shows an example of a 100W half-bridge power converter controlled by the LM5035A. The operating input voltage range (V_{PWR}) is 36V to 75V, and the output voltage is 3.3V. The output current capability is 30 Amps. Current sense transformer T2 provides information to the CS pin for current limit protection. The error amplifier and reference, U3 and U5 respectively, provide voltage feedback via opto-coupler U4. Synchronous rectifiers Q4, Q5, Q6 and Q7 minimize rectification losses in the secondary. An auxiliary winding on transformer T1 provides power to the LM5035A VCC pin when the output is in regulation. The input voltage UVLO thresholds are ≅34V for increasing V_{PWR}, and ≅32V for decreasing V_{PWR}. The circuit can be shut down by driving the ON/OFF input (J2) below 1.25V with an open-collector or open-drain circuit. An external synchronizing frequency can be applied through a 100pF capacitor to the RT input (U1 pin 5). The regulator output is current limited at ≅34A.

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Table 2. Differences between LM5035, LM5035A, LM5035A-1, LM5035B, and LM5035C(1)(2)

Performance Feature:		LM5035	LM5035A	LM5035A-1	LM5035B	LM5035C
Sync Rectifier Dead-time Ratio (T1:T2)		2:1	3:1	3:1	3:1	3:1
Soft-start: Hiccup Mode Charging Current		50µA:1µA	100µA:1µA	100µA:1µA	100µA:1µA	100µA:1µA
Bootstrap (HB-HS) Under-Voltage Lockout		5V	3.9V	3.9V	3.9V	3.9V
Start-up Regulator Current		20mA (min)	25mA (min)	25mA (min)	40mA (min)	40mA (min)
SR State in UVLO Shutdown and Hiccup Current Limit		High	High	High	Low	Low
HO,LO On-Time at Max Duty Cycle		0.5*T-T1–70 ns	0.5*T-T1–70 ns	0.5*T-T1–70 ns	0.5*T-T1	0.5*T-T1
Soft-Stop after UVLO	HO,LO	Yes	Yes	Yes	Yes	No
	SR1,2	Yes	Yes	Yes	No	No
SR1, SR2 VOH (high state output)		VCC	VCC	VCC	VCC	REF (5V)
Package		HTSSOP-20, WQFN-24	HTSSOP-20, WQFN-24	HTSSOP-28	HTSSOP–20, WQFN-24	HTSSOP-20, WQFN-24

(1) T1 = Delay from SR1, SR2 to leading edge of HO, LO
(2) T = Period of HO or LO

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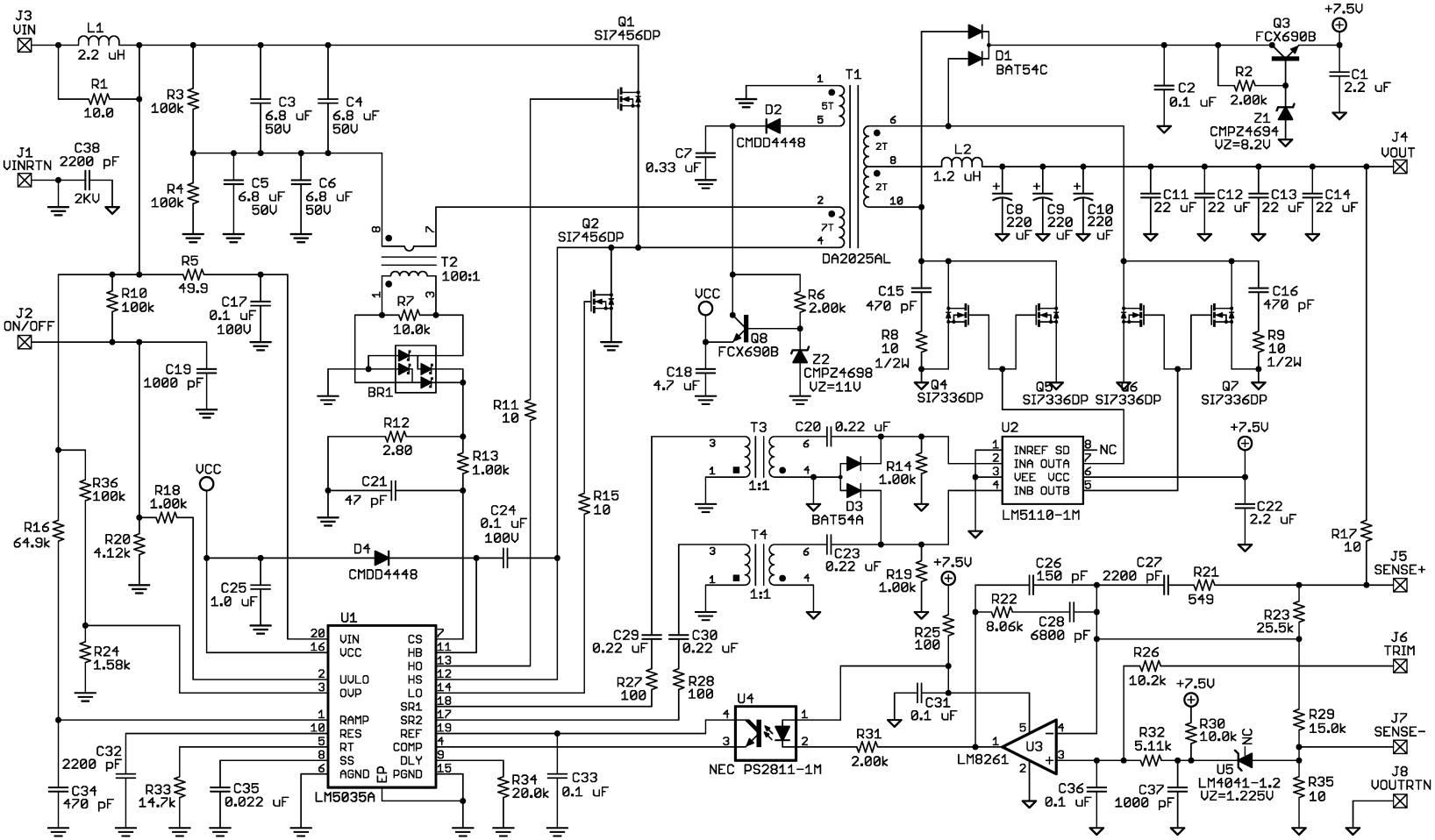


Figure 29. Evaluation Board Schematic

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	29

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5035AMH-1/NOPB	LIFEBUY	HTSSOP	PWP	28		TBD	Call TI	Call TI		LM5035 AMH-1	
LM5035AMH/NOPB	LIFEBUY	HTSSOP	PWP	20		TBD	Call TI	Call TI	-40 to 125	LM5035 AMH	
LM5035AMHX-1/NOPB	LIFEBUY	HTSSOP	PWP	28		TBD	Call TI	Call TI		LM5035 AMH-1	
LM5035AMHX/NOPB	LIFEBUY	HTSSOP	PWP	20		TBD	Call TI	Call TI	-40 to 125	LM5035 AMH	
LM5035ASQ/NOPB	LIFEBUY	WQFN	NHZ	24		TBD	Call TI	Call TI	-40 to 125	5035ASQ	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

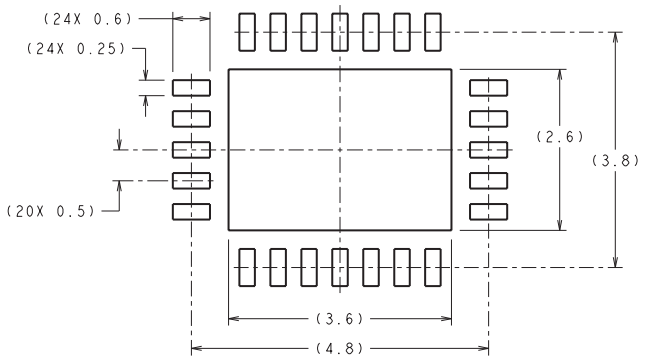
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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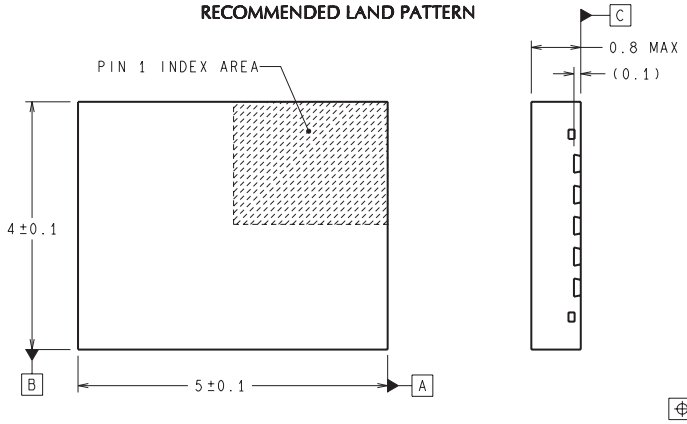
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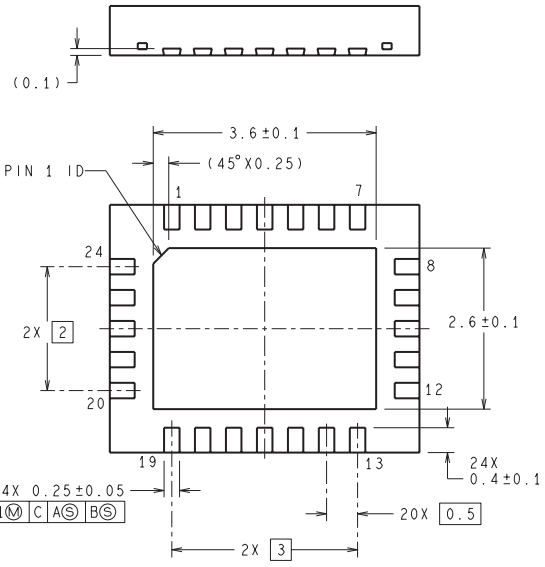
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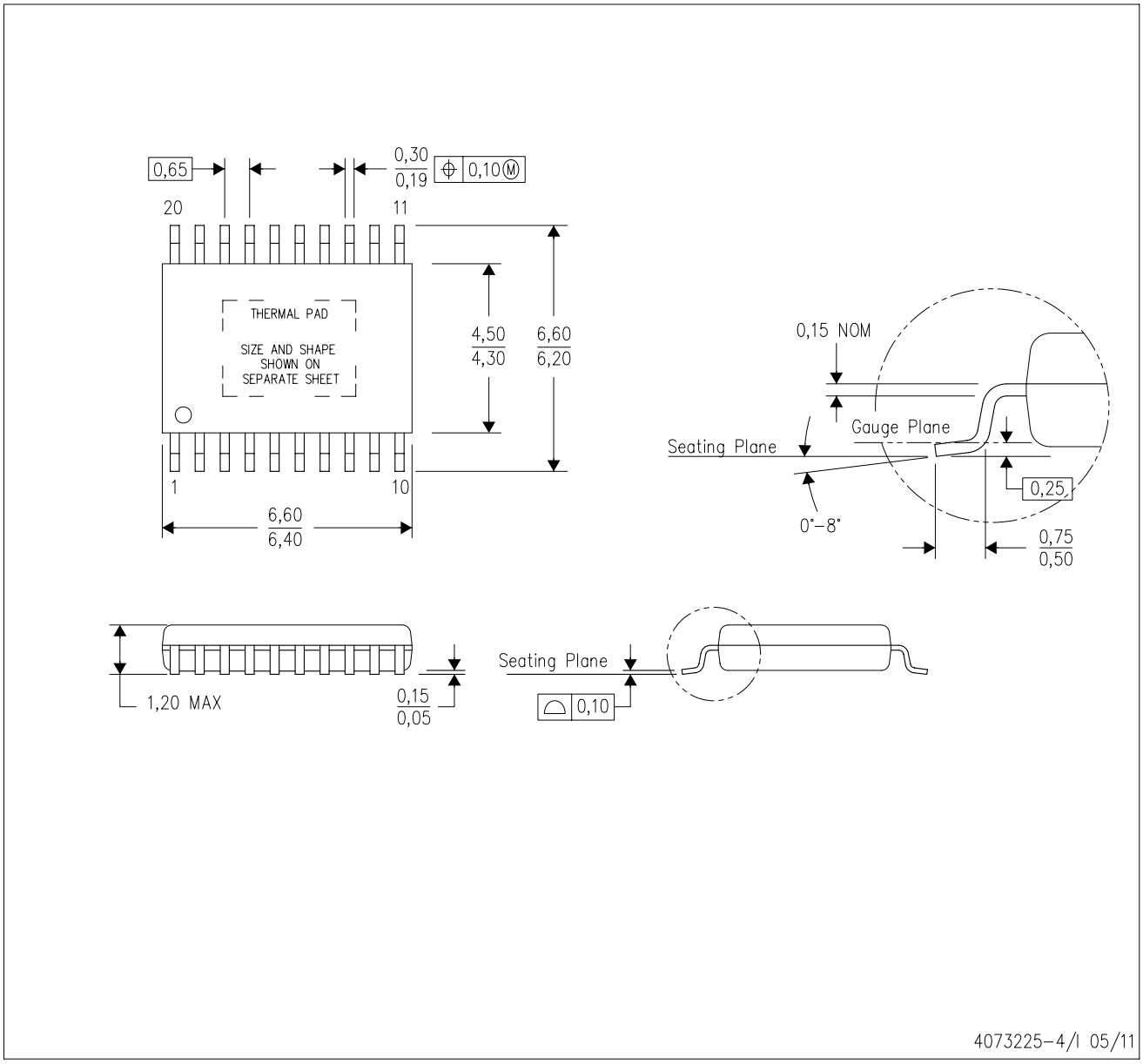
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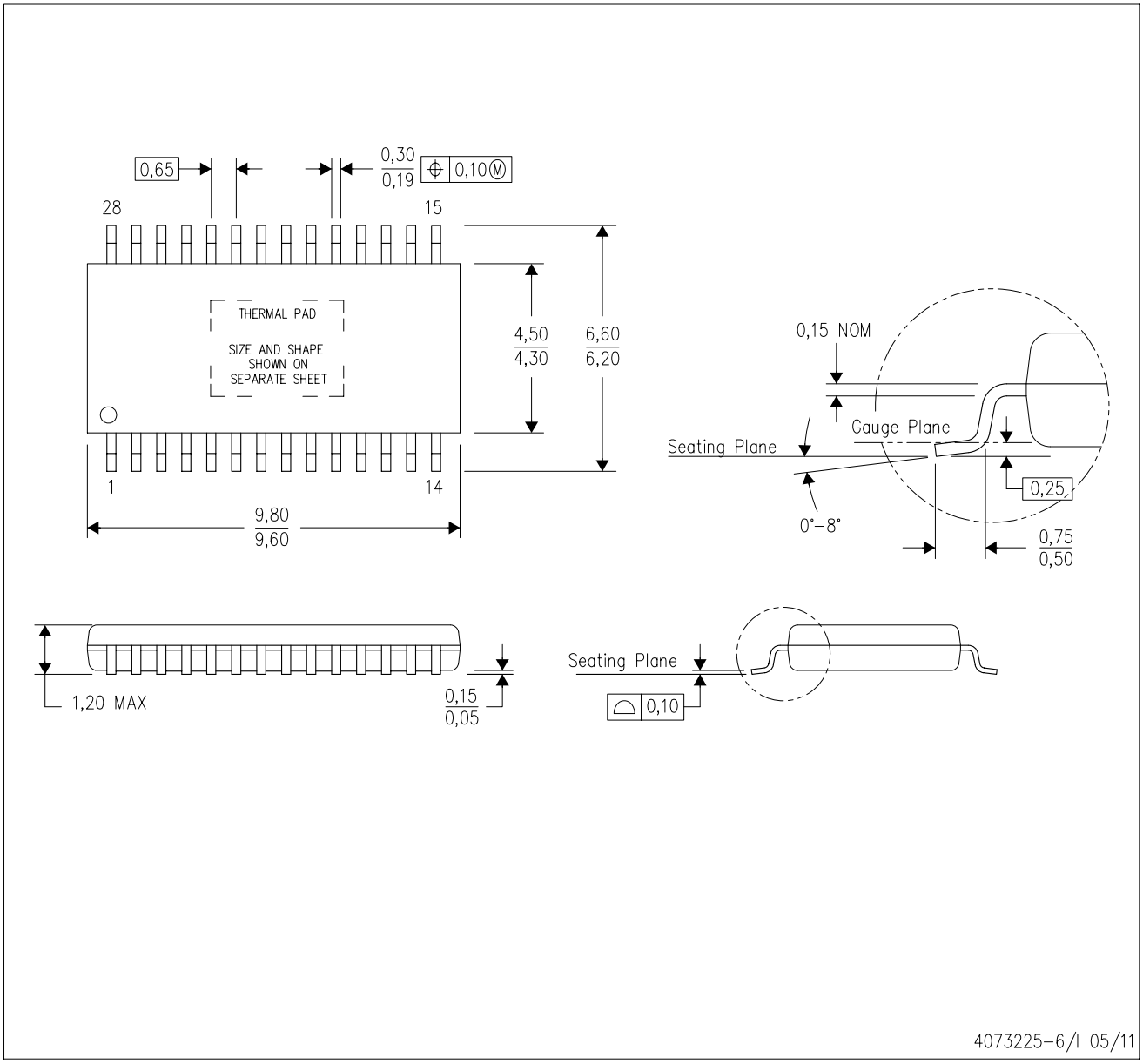
PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
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B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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